IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Gunnar Wetzker, et al.
For	:	RECEIVER FOR RECEIVING FREQUENCY SIGNALS USING DELTA-SIGMA MODULATORS
Serial No.	:	10/564,293
Filed	:	January 10, 2006
Art Unit	:	2611
Examiner	:	Eboni N. Giles
Atty. Docket	:	NL 030813
Confirmation No.	:	6995

REPLY BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed on December 30, 2009.

I. STATUS OF CLAIMS

Claims 1-9 and 11 are on appeal.

Claims 1-9 and 11 are pending.

No claims are allowed.

Claims 1-9 and 11 are rejected.

Claim 10 is canceled.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

A. The rejection of claims 1, 2, and 5-9 under 35 U.S.C. § 103(a), as being unpatentable over Pub. No. US2004/0057534 ("*Masenten*") in view of Pub. No. US2004/0210801 ("*Prasad*"). Office Action at pp. 2-6.

B. The rejection of claims 3 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Masenten* in view of *Prasad*, further in view of U.S. Patent No. 7,194,036 ("*Melanson*"). Office Action at p. 6.

C. The rejection of claim 4 under 35 U.S.C. § 103(a) as being unpatentable over *Masenten* in view of *Prasad* and further in view of U.S. Patent No. 7,130,327 to ("*Robinson*"). Office Action at pp. 6-7.

D. The rejection of claim 11 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Masenten* in view of *Prasad* and further in view of U.S. Patent No. 6,225,928 ("*Green*"). Office Action at pp. 7-8.

III. ARGUMENTS

A. Rejections of Claims 1, 2, and 5 - 9

1. The Examiner's Assertion That the References Lack the Claimed Decimator Receiving a Feedback Signal Is Not Responsive to Appellant's Brief and Contends an Improper Interpretation of the Claim Language

Appellant's Brief set forth arguments that the Examiner erred in failing to give weight to the claim 1 and 7 language: "decimator receiving a feedback signal from a time-control loop having a loop quantizer and a loop filter." Appeal Brief at pp. 6-7. Appellant's Brief argued that the error is fatal to the rejection; nowhere in the combined disclosures of *Masenten* and *Prasad* is there a teaching or suggestion toward the language the Examiner omitted to consider, namely a "decimator "receiving a feedback signal from a time-control loop having a loop quantizer and a loop filter." *Id.*

Appellant respectfully submits the Examiner's Answer does not respond to Appellant's showing of this error, and instead states – correctly, but citing the wrong basis – that claims 1 and 7 do "not require the decimation filter in the feedback loop" but contends – incorrectly – that FIG. 3 of Appellant's application is a basis for that statement. Examiner's Answer, at p. 12.

As for the correct portion of the Examiner's statement that claims 1 and 7 do not require a decimation filter in the feedback loop, the plain language of claims 1 and 7 indeed *defines* the decimation filter as *not* being *in* the feedback loop.

The Examiner's citation to FIG. 3, however, as supporting the statement that claim 1 "does not require the decimation filter in the feedback filter" is *incorrect.* It is incorrect because claim 1 is *not* drawn to FIG. 3. Claim 1 is drawn to FIG. 5. FIG. 3 does *not* support claim 1; *it is FIG. 5 that supports claim 1.*

Appellant respectfully submits that the plain meaning of the claim 1 language shows that logically the claim *cannot* encompass the decimation filter being *in* the feedback loop, and additionally shows the error in the Examiner's Answer's citing FIG. 3.

More particularly, referring to claim 1, the combination includes a receiving stage, a mixing stage connected to the receiving stage, a modulating stage that delta sigma modulates the output of the mixing stage, and a filtering stage coupled to the modulating stage that filters its delta sigma modulate output. Claim 1 at lines 2-8. The claim further recites the filtering stage as having a decimator, and recites the decimator as receiving an output signal from a time control loop having a loop quantizer and a loop filter. Claim 1 at lines 8-10. The decimator cannot receive a feedback signal from a feedback loop and be part of the feedback loop.

Appellant's FIG. 5, and paragraph [0055] of the printed version of the specification show structure within the meaning of claim 1, illustrating the decimator [Fig. 5: 52], not in the feedback loop, controlled by an output signal generated by the quantizer [Fig. 5: 23] that is within the feedback loop.

Appellant respectfully submits the Examiner' Answer shows no facts rebutting Appellant's argument that *Masenten* and *Prasad* have no teaching of, or suggestion toward the claim 1 "decimator "receiving a feedback signal from a time-control loop having a loop quantizer and a loop filter."

2. The Examiner's Answer Alleging That the References Teach the Claimed Time-Control Loop Having a Loop Quantizer and a Loop Filter Asserts a New Argument, Based on an Improper Interpretation of the Claim Language

Appellant has submitted arguments and facts showing error in the Examiner's position contending that *Masenten* in view of *Prasad* shows structure meeting the recitation of "a time control loop having a loop quantizer and a loop filter" in claim 1. Appeal Brief, at pp. 6-7.

The Examiner Answer, in response, alleges that the "time control loop is identical to Fig. 3, page 8 of the appellant's disclosure." Examiner's Answer, at p. 12.

Appellant respectfully submits the Examiner's Answer is in error. Claim 1 is not drawn to, and is not supported by, Appellant's FIG. 3. Claim 1 is drawn to and supported by Appellant's FIG. 5. Appellant respectfully submits that the Examiner's interpretation must either omit words of the claim, or interpret the specification and figures in a manner not consistent with their disclosure as it would be understood by a person of ordinary skill in the art.

As recited by the claim, the time control loop comprises a loop filter (e.g., Fig. 5: 22) and a quantizer (e.g., Fig. 5: 23). Appellant's FIG. 5 and, for example, Paragraph [0054] of the printed version of Appellant's specification provide clear support for this claim 1 language. Appellant's FIG. 3, which is cited by the Examiner as supporting claim 1, does not.

B. Rejection of Claim 11

1. **The Examiner's Answer to Appellant's Showing That the References Lack "An Adder That Combines an Input Signal with a Feedback Signal" Asserts a New Argument that is Based on an Improper Interpretation of the Claim Language**

Appellant has submitted arguments and supporting facts showing error in the Examiner's stated position that *Masenten* in view of *Prasad*, further in view of *Green*, shows structure meeting the recitation of "an adder that combines an input signal with a feedback signal, thereby producing a sum" in claim 11. Appeal Brief, at p. 10.

The Examiner's Answer alleges that *Green* provides two adders in the context of a $\Delta\Sigma$ ADC. Examiner's Answer, at pp. 14-16. Appellant respectfully responds that the Examiner's Answer is in error, as *Green's* teachings are inapplicable to *Masenten* in view of *Prasad* because *Green's* adders do not appear in the context of a loop filter. Moreover, *Green* does not remedy the deficiencies of *Masenten* in view of

Prasad described at subsection B above, as the Office Action fails to provide a loop filter with a loop quantizer in a time-control loop.

2. The Examiner's Answer to Appellant's Showing That the References Lack "An Inverse Z Block That Receives the Sum and Produces the Feedback Signal" is a New Argument and Is Based on Error, Applying an Overly Broad Interpretation to Claim Language

Appellant submitted argument and supporting facts showing errors in the Examiner's position that *Masenten* in view of *Prasad*, further in view of *Green*, shows structure meeting the recitation of "an inverse z block that receives the sum and produces the feedback signal" in claim 11. Appeal Brief, at p. 10.

The Examiner's Answer alleges that *Green* provides a delay block as an inverse z block in the context of a ΔΣ ADC. Examiner's Answer, at pp. 14-16. Appellant respectfully responds that the Examiner's Answer is in error, and submits that *Green's* teachings are inapplicable to *Masenten* in view of *Prasad* because *Green's* delay block does not appear in the context of a loop filter. The Examiner cites *Green* merely as a teaching of a delay block, and identifies no motivation for combining *Green* with the other references to achieve Appellant's claim 11. Moreover, *Green* does not remedy the deficiencies of *Masenten* in view of *Prasad* described above, for reasons including *Green's* lack of loop filter with a loop quantizer in a time-control loop.

3. The Examiner's Answer to Appellant's Showing That the References Lack "a Gain Block That Processes the Feedback Signal to Produce an Output Signal" is a New Argument Applying an Overly Broad Interpretation to the Claim Language

Appellant submitted argument and supporting facts showing errors in the Examiner's position that *Masenten* in view of *Prasad*, further in view of *Green*, shows structure meeting the recitation of "a gain block that processes the feedback signal to produce an output signal that is sent to the loop quantizer" in claim 11. Appeal Brief, at p. 10.

The Examiner's Answer alleges that *Green* provides a DAC having a desired gain as a gain block in the context of a $\Delta\Sigma$ ADC. Examiner's Answer, at pp. 14-16. Appellant respectfully submits that *Green's* teaching cited by the Examiner is taken out of its original context, and is inapplicable to *Masenten* in view of *Prasad* because *Green's* DAC does not appear in the context of a loop filter. Moreover, *Green* does not remedy the deficiencies of *Masenten* in view of *Prasad* described above, as the Office Action fails to provide a loop filter with a loop quantizer in a time-control loop.

CONCLUSION

For the reasons set forth herein and in the Appeal Brief, Appellant respectfully requests that this Honorable Board reverse the rejections of the claims under 35 U.S.C. § 103(a).

Respectfully submitted,
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